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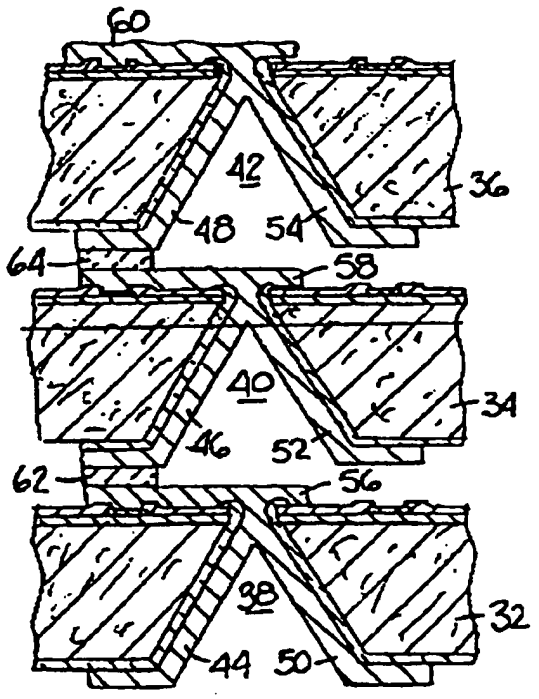
(54) Title: APPARATUS AND METHOD OF MANUFACTURING STACKED WAFER ARRAY

(57) Abstract

A semiconductor device utilizing stacked, undiced wafers and a process of manufacturing the same. A set of stacked undiced wafers (36, 34, 32) include through-holes (42, 40, 38) which are partially or entirely coated with an electrically conductive material (48, 46, 44) which extends out of the through-hole and onto the wafer surface to form a conductive pad (60, 58, 56). The pad on top of one wafer contacts the pad on the bottom of an adjacent wafer to establish electrical communication therebetween. The conductive material coats, but does not fill, each hole, so that a minimum of electrical capacitance is introduced to the connection. The holes are anisotropically etched.



APPARATUS AND METHOD OF MANUFACTURING STACKED WAFER ARRAY

FIELD OF THE INVENTION

The present invention is in the field of semiconductor wafer arrays wherein an undiced wafer is arrayed with at least one other undiced wafer to form a "stack". In particular, the present invention relates to an apparatus of stacked wafers having a novel system for making electrical connections therebetween, and a method of manufacturing and assembling the wafers to produce such electrical connectors using plated through-hole contacts.

BACKGROUND OF THE INVENTION

Computer processing and storage devices have for many years been fabricated from wafers of semiconductor materials which include large numbers of integrated transistor circuits. The wafers have traditionally comprised many connected chips. The manufactured wafer is "diced" or cut into these chips, and the diced chips are adhered to carriers and interconnected by fine wiring.

This process of manufacturing finished chips is somewhat expensive. Moreover, the fine wiring and the wiring connections tend to be unreliable, and the length of the wires required to make the necessary interconnections among various chips tends to result in undesirable signal delays. The signal delays have become an increasing problem in recent years as the maximum speed of the systems in which the devices are used has steadily increased.

One approach in the prior art to increasing the memory density of semiconductor devices has been the straightforward approach of reducing the standard package size of memory chips, as by using small outline packages (SOPs) or very small outline packages (TSOPs). The reduced-sized chips are then installed on PC modules that plug into a mother board such as a small

inline memory module (SIMM). While such an approach is effective, it still does not result in a memory density as high as desired.

More recently, there has been an attempt to utilize entire wafers intact rather than dicing them into individual chips that are reconnected. Such approaches have been dubbed "wafer scale integration" (WSI). Such WSI approaches have included connecting the undiced chips that test good in a wafer with discreet wiring; however, that approach has presented technical difficulties associated with the discreet wiring and has resulted in poor yields and high costs. Another approach also utilizes undiced wafers which are interconnected, but the interconnection is achieved by a software mapping scheme to bypass the bad chips rather than using fine wiring. An undiced wafer mapped out with the mapping scheme is then placed on each side of a PC board. A serial access through intermediate chips is used, which produces rather long signal delays due to the long path of the serial access.

In yet another approach, intact wafers of dynamic random access memories (DRAMs) are interconnected by bundles of gold wires threaded through a set of through-holes etched into the wafers, to allow the wafers to be stacked one on top of the other to produce a very high packing density. The pliability of the gold wires can accommodate relative motion between the stacked wafers caused by variable thermal expansion. While this approach provides very high memory densities, it is prohibitively expensive because it requires careful and exact wire placement and entails high cost and handling problems associated with automated equipment used for that placement.

The general idea of interconnecting chips in intact wafers rather than dicing them and reconnecting them electrically is still a good one, since the cost of a typical chip such as a 16-Mbit DRAM in wafer form

is a fraction of the cost of the same chip mounted in packaged form. The main obstacle to that idea is still making the electrical interconnections in a manner that is reliable, inexpensive and does not result in long signal delays. If the electrical interconnection problem could be overcome, a semiconductor bulk memory constructed of undiced wafers could be orders of magnitude faster than hard disc memory. Further it would be more reliable, since hard disc memory devices are notoriously complex mechanical devices while semiconductor memories utilize no moving parts at all.

A stacked wafer design is taught in U.S. Patent No. 5,229,647 by Gnadinger, the contents of which are hereby incorporated by reference. In the Gnadinger patent, interconnections between wafers are established using bumps and through-holes aligned with metal pads. The bumps on one wafer contact with metal pads on a mating wafer. Serial addressing and data access are used for the memory units to minimize the number of connections necessary between adjoining wafers.

A limitation to the Gnadinger device is that it teaches a simple contact between adjacent wafers to establish electrical communication therebetween, without any mechanical bonding. Mechanical bonding is avoided to allow differential thermal expansion in adjacent wafers without breaking the electrical connection. While that does solve the problem of differential thermal expansion in adjacent wafers, it also results in a less certain electrical connection, and greater resistance in the circuit. Also, such an approach becomes infeasible when multiple contacts must be made, due to the amount of force required to maintain such contacts.

Also, the preferred embodiment of the Gnadinger patent teaches completely filling the through-hole with metal to carry a signal from one side

of the wafer to the opposite side. It has now been discovered, however, that a fully metalized through-hole is undesirable from an electrical standpoint because it results in an undesirably large electrical capacitance due to its relatively large dimensions. It is true that a fully metalized through-hole has desirable low resistivity characteristics, but the resistance of the metal typically used for the metalization (usually gold) is sufficiently low that resistivity is not normally a limiting factor.

It would therefore be desirable to design a device and a method for manufacturing the same, wherein intact wafers can be stacked to produce high-density memory systems, using metalized through-holes for electrical contacts, but without prohibitively high capacitance or other undesirable electrical characteristics.

SUMMARY OF THE INVENTION

The present invention includes an apparatus and method for manufacturing the same, wherein standard silicon CMOS and/or bi-polar technology wafers (or, for that matter, wafers utilizing other technologies such as GaAs, ferroelectrics, etc.) are assembled in stacked or arrayed configurations. The electrical interconnections between the layers are accomplished using plated through-hole contacts. Such through-hole contacts offer the advantage that the average signal line length and the maximum number of interconnections per unit area does not depend upon the chip area. This is in contrast to the alternative approach where all signals are drawn to the edges of the stack or vertical interconnection, resulting in the average signal line length and the maximum number of interconnections being roughly proportion to the square root of the area of each wafer layer.

The through-holes are anisotropically etched

through the wafer layer and insulated. A conducting layer, preferably of gold, is electroplated or otherwise placed in the through-hole to feed the electrical signal from the conventional circuitry on the wafer face via a standard contact pad to the back of the substrate.

Several chips, blocks of chips or even entire intact wafers carrying plated through-holes are then stacked or arrayed one on top of the other and joined by means of reflow soldering. Co-integrated thermal contacts between the silicon layers may be employed to provide adequate thermal relief for the system to prevent undue differential thermal expansion. The entire stacked or arrayed assembly is mounted on a base plate with additional components and wiring. The base plate is fabricated with standard thick/thin film technologies as used in fabricating hybrids and MCMs, and the entire system is hermetically encapsulated.

The through-hole contacts are formed by additional processing after the conventional IC fabrication is completed. No modifications to the standard CMOS, bi-polar or other processes are necessary. The anisotropically etched through-holes are etched from the back of the wafer, which results in very small openings on the wafer face holding the integrated circuits; thus, only a small portion of the silicon area must be sacrificed for each vertical interconnection. An oxide serves as the etch stop on the wafer front. The etching is carried out in a KOH solution at elevated temperatures, using a fixture to seal the wafer face against the etchant; the seal protects the wafer face, in particular the aluminum metalization, from being attacked by the KOH. Moreover, using the fixture, the alkaline metal-contaminated zone is limited to the wafer back where it can be easily removed. After stripping the etch stop membrane, the side walls of the holes are protected

with another oxide layer, and the electrical interconnection is applied with a selective electrode deposition of gold.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a final assembly of stacked intact wafers in accordance with the present invention.

FIG. 2 shows a side sectional view of a set of stacked wafers, showing the electrical interconnections thereof.

FIG. 3A is a pictorial view of a plated through-hole in accordance with the present invention.

FIG. 3B is a pictorial view of a plated through-hole in accordance with an alternative embodiment of the invention.

FIG. 3C is a pictorial view of a plated through-hole in accordance with an alternative embodiment of the invention.

FIG. 3D is a pictorial view of a plated through-hole in accordance with an alternative embodiment of the invention.

FIGs. 4A-4P show steps in a process in accordance with the present invention.

FIG. 5 shows a side sectional view of a device used in practicing the present invention.

FIG. 6 shows a side sectional view of another device used in practicing the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A final assembly of a high density storage system utilizing stacked intact wafers in accordance with the present invention is shown in FIG. 1. The assembly 10 includes an enclosure 12 such as a metal case mounted on a base plate 14. A wiring plane 18 is positioned on the base plate 14. A plurality of silicon wafers 16 are stacked or arrayed within the space defined by the enclosure 12 and base plate 14.

FIG. 2 shows a detail of three wafer layers, 32, 34 and 36 in stacked configuration. As evident from the illustration of FIG. 2, each of the three wafer layers 32, 34 and 36 includes a through-hole 38, 40 and 42, respectively, which is plated with an electrical conductor 44, 46 and 48, respectively. Each electrical conductor 44, 46 and 48 includes a bottom side portion, 50, 52 and 54, which plates a portion of the through-holes 38, 40 and 42, respectively, and a pad portion 56, 58 and 60 to make contact with the through-hole portion of the adjacent wafer as well as with a micro circuit located on the wafer face. The pad of each electrical conductor contacts makes electrical communication with the plated through-hole portion of the adjacent wafer by a in-flow solder joint 62 and 64. It can be appreciated that, while only three wafers are shown in the depiction of FIG. 2, the assembly could instead include only two wafers or any number of wafers greater than three or only one wafer on a base plate.

The through-hole 38, 40 and 42 of FIG. 2 may be plated completely with the electrical conductor or may be only partially plated. Various optional plating approaches are depicted in pictorial views of the through-holes stacked in FIGs. 3A, 3B and 3C. FIG. 3A shows a fully metalized through-hole, in which the wafer back side is fully metalized in the form of a electrical conductor electroplated thereon. The electrical conductor 82 extends from the pyramid of the shaped through-hole surface to the wafer back side surface where it forms a pad 84 to contact the adjacent wafer (not shown).

In the embodiment of FIG. 3B, the through-hole surface 74 is partially metalized with partial metal plating 70 which extends onto the wafer back side to form an electrical contact pad 72 for electrical communication with the adjacent wafer (not shown). In

the embodiment of FIG. 3C, the through-hole surface 90 is once again partially metalized by an electrical conductor plating 92. The electrical conducting electroplate 92 extends around the apex of the pyramid of the shaped through-hole surface 90, and includes a tab 94 extending from the apex to the backside surface which terminates in a pad 96 in communication with the adjacent wafer (not shown). The goal of the designs are to reduce the surface area of the electroplated electrical conduits in order to minimize capacitance with respect to a fully metalized through-hole. Furthermore, the production costs are reduced because of the reduced mass of the electroplated gold.

The device of the present invention may utilize multiple independent circuit pathways as shown in FIG. 3D. As shown in that figure, the through-holes may include several electrical conducting electroplate surfaces or "traces." In that manner, a single through-hole can be used to accommodate several electrical connections. Each trace on each side of the through-hole terminates in a conductive pad for contact with an adjacent wafer in the manner of the single trace design already described.

Next described is the process for manufacturing the electroplated through-holes, by reference to FIGs. 4A-4P. Initially, a conventional CMOS process is carried out without any special modification. The backside of the wafer needs no special treatment, but can be covered by any combination of oxides and nitrides. A typical CMOS processed wafer 110 is shown in FIG. 4A. The wafer 100 includes a silicon body 101 having an unfinished back side 102 coated with oxides and/or nitrides 103. The front side includes a field oxide/insulation oxide layer 104, a passivation layer 105 and a series of pads 106.

FIG. 4B shows the application of a protective

layer 112 of oxide or nitride to a thickness of 3,000 - 5,000 angstroms for the purpose of protecting the uncovered aluminum pads from mechanical or chemical damage. Mechanical damage is common in the form of scratches and abrasions due to the wafer 110 being placed repeatedly upside down on processing equipment. Chemical damage is possible due to contact with traces of the etchant. The etchant used in the preferred embodiment - potassium hydroxide - is highly corrosive to aluminum. The oxide or nitride protective layer 112 must be thick enough to cover all hillocks and edges of the aluminum.

The oxide and/or nitride layer 103 (see FIG. 4A) on the back side 102 of the wafer 100 is stripped either wet chemically or in a plasma etcher. Because the wet chemical approach requires front side protection (such as a photoresist layer), the plasma method is preferable. In addition, the back side 102 should be made as planar and defect-free as possible. A low defect density is important since anisotropic etching is crystal orientation dependent. Defects in the crystal increase the etch rate significantly and cause poor control over the etch pit dimensions. Likewise, surface planarity is critical for a uniform, defect-free coverage with PECVD films which are later deposited on the wafer backside 102. A planarization back etching can be accomplished using mechanically assisted isotropic silicon back etch (so called chemical polishing). Such an approach results in a defect-free mirror-like surface, and the method is well established, inexpensive and straight forward. Further, no wafer front side protection is needed. Alternatively, a brief potassium hydroxide etch may be used for planarizing the wafer back side 102. It is believed that a potassium hydroxide etch is not as desirable as mechanically assisted isotropic silicon etching for this purpose, since the resulting planarity

is less than perfect and requires durable processing efforts.

The next step is deposition of a KOH etch mask 122, as shown in FIG. 4C on the planarized wafer back side 102. The etch mask 122 is a PECVD nitride which serves as a mask for the subsequent KOH etching of through-holes in the wafer. The minimum thickness of the mask 122 depends on the nitride etch rate in KOH; for 700 μm thick wafers, the mask typically needs to have a thickness of 0.5 - 1.0 μm.

After the KOH etch mask is applied to the wafer back side 102, a photoresist layer 123 is applied over the KOH etch mask 122 as shown in FIG. 4D for the purpose of defining the interconnection holes.

The next step, as shown in FIG. 4E is to nitride etch the etch mask 122 and then strip the photoresist 123. Preferably, the nitride etch is to isotropically etch 1 - 2 μm deep into the silicon after the nitride has been removed. This can be accomplished with a pure SF_6 plasma driven at low power. A properly etched nitride will result in an undercut at the nitride edges. FIG. 4F shows the results of anisotropic etching of the through-holes using potassium hydroxide. The preferred embodiment utilizes a KOH concentration of 4 - 6 M at about 95°C. An etch rate of approximately 150 μm per hour is achieved; because the wafer 110 is approximately 500 - 700 μm thick, the total etch time is on the order of 4 1/2 hours. The end point of the etching can easily be detected by the cessation of hydrogen bubbles produced by the reaction of OH with silicon.

It is important to protect the wafer front side and edges from the KOH etchant. FIG. 5 shows a cross-sectional view of a mechanical fixture for that purpose. The fixture 210 includes a stainless steel base plate 212, an overplate 214 and a PTFE insert 216. The wafer 110 is mounted on the PTFE insert 216, top

side down, and the overplate 214 is attached to the base plate 212. A set of O-ring seals 218 and 220 seal the front side from exposure, so that the KOH etchant is exposed to only the back side.

The next step is to strip the mask on the wafer backside 102 and the oxide membranes 112 on the wafer front side. The fact that the KOH etch mask consists of non-stoichiometric PECVD nitride allows it to be stripped in buffered hydrofluoric acid. The front side of the wafer must be protected during this operation, since the etchant otherwise attacks both the passivation and the underlying layers such as the intermetal oxides. Front side protection can be accomplished using a photoresist layer 131 which may be spun on as shown in FIG. 4G.

The front side protection layer 112 is no longer necessary at this point, and therefore may be stripped in a BHF (=Buffered HF) or plasma stripping operation as shown in FIG. 4H.

The next step is a substrate back etch step also shown in FIG. 4H. The purpose of this step is to remove roughly 1 - 2 μm of silicon on the wafer back side. This removes any remaining contamination of alkaline metals on the side wall of the etch pits, and also conditions the edge of the edge pit on the wafer front side for a conformal insulator coverage. FIG. 4I shows before and after views of the border between the etch pit and the oxide layer illustrating the conditioning of the edge.

The next step is to deposit an interconnection insulator 170 as shown in FIG. 4J. The wafer 110 is placed upside down in a PECVD reactor, and care is taken to prevent oxide deposits on the wafer front side which could insulate the electrical pads.

FIG. 4K shows the sputter deposition of TiW as a diffusion barrier and Au as a seed layer 172.

The next step is probimide spin-on. The goal

of this step is to cover both sides of the wafer 110 with PROBIMIDE 348 or PROBIMIDE 7020 brand of Ciba-Geigy. Proper coverage of the wafer back side is not difficult, since the probimide has a very high viscosity and planarizes even etch pits. The major difficulty is in the fact that there are holes in the wafers in the form of the through-holes, and a standard spin-on procedure using a vacuum chuck causes the probimide to be sucked through the holes. FIG. 6 shows a special chuck which is used to overcome this difficulty. The special chuck 310 holds the wafer 110 in place at the wafer periphery using pins 312. The probimide is first spun onto the wafer back side to planarize the etch pits. Surface tension prevents it from flowing through the holes onto the wafer front side, as shown in FIG. 4M. After the soft bake step, the probimide is quite tough and all holes in the wafer are thereby closed, and the front side of the wafer can then be coated using a standard vacuum chuck.

FIG. 4N is the lithography step to define the pad sides. Both sides of the wafer 110 are exposed sequentially utilizing conventional lithographic methods. Wafer handling at this point does not pose special problems since the probimide is fairly tough and invulnerable. Development of the probimide is carried out in an ultrasonic bath. Finally, the wafer 110 is electroplated to a thickness 190 of about 25 μm as shown in FIG. 4O, and the plating mask and seed layers are stripped as shown in FIG. 4P.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising: a plurality of semiconductor wafers arranged adjacently in a stack, each wafer having at least one through-hole with a top side and a bottom side and a hole wall connecting the top side to the bottom side and with an electrically conductive material coated onto at least a portion of the wall whereby the conductive material does not fill the through-hole, the wafers arranged in said stack whereby the conductive material at the top side of a wafer contacts and establishes electrical communication with the conductive material at the bottom side of an adjacent wafer.

2. The semiconductor device of claim 1, wherein the through-hole has an opening at the top side and a wider opening at the bottom side.

3. The semiconductor device of claim 1, wherein said conductive material coats some but not all of the hole wall.

4. The semiconductor device of claim 1, wherein the wafer includes a wafer top side adjacent the hole top side and a wafer bottom side adjacent the hole bottom side, and wherein the conductive material extends through the hole top side and onto the wafer top side to form a top conductive pad and through the hole bottom side and onto the wafer bottom side to form a bottom conductive pad, the top conductive pad of a wafer being in contact and electrical communication with the bottom conductive pad of an adjacent wafer.

5. The semiconductor device of claim 4, wherein the top conductive pad of a wafer is soldered to the bottom conductive pad of an adjacent wafer.

6. The semiconductor device of claim 1, wherein the hole wall is partially coated with conductive material in a plurality of separate electrical pathways.

7. A method for producing a semiconductor device, comprising: forming holes through a plurality of wafers, each hole having a hole wall that extends from a hole top side to a hole bottom side; at least partially coating the hole wall with an electrically conductive material whereby the conductive material does not fill the hole; and stacking said wafers adjacent to one another whereby the conductive material at a hole top side of a wafer is in contact and electrical communication with the conductive material at a hole bottom side of an adjacent wafer.

8. The method of claim 7, wherein the said coating step includes substantially completely coating the hole wall with the conductive material.

9. The method of claim 7, wherein the coating step includes partially but not completely coating the hole wall.

10. The method of claim 7, wherein the wafer has a wafer top side adjacent the hole top side and a wafer bottom side adjacent the hole bottom side, and where the coating step includes extending the conductive material from said hole wall through the hole top side and onto the wafer top side to form a top pad and from said hole wall through the hole bottom side and onto the wafer bottom side to form a bottom pad, and said stacking step includes contacting a top pad of a wafer with a bottom pad of an adjacent wafer to establish electrical communication therebetween.

11. The method of claim 7, wherein said forming a hole step includes etching the wafer.

12. The method of claim 11, wherein said forming a hole step includes applying a mask to a bottom side of the wafer, and etching the wafer through voids in the mask to form a hole having an opening at an end that is larger than an opening at an opposite end.

13. The method of claim 12, wherein the

voids in the mask are produced by applying a photoresist layer over the mask, and etching the mask through the photoresist layer.

14. The method of claim 13, wherein the coating step includes applying a probimide coating to the hole wall and selectively removing the probimide coating to expose a seed layer for application of the conductive coating.

15. The method of claim 14, wherein the stacking step includes soldering the conductive material of a wafer to the conductive material of an adjacent wafer.

16. The method of claim 7, wherein said at least partially coating step includes establishing a plurality of separate electrical pathways in said conductive materials through said hole.

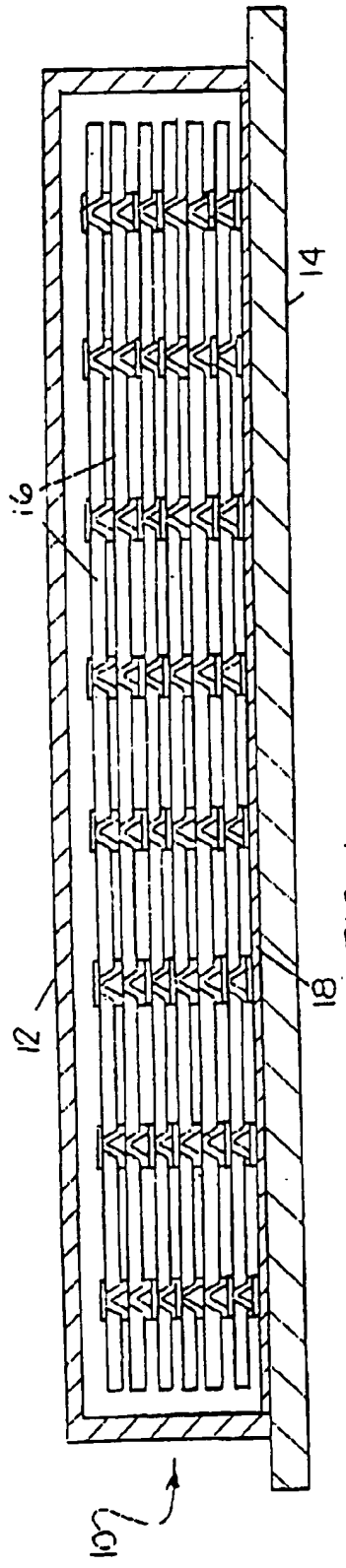


FIG. 1

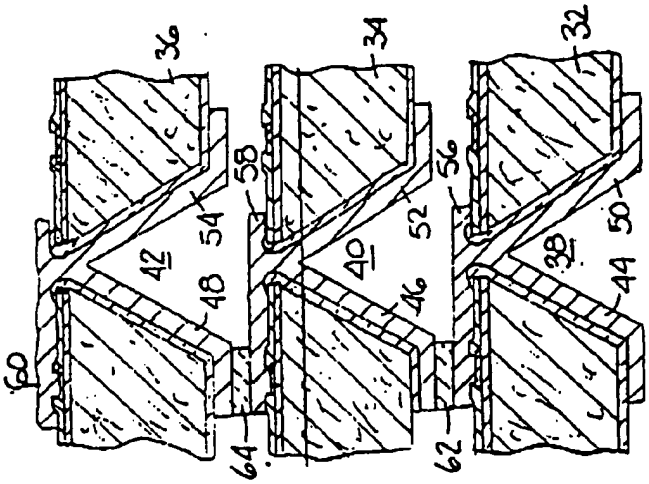


FIG. 2

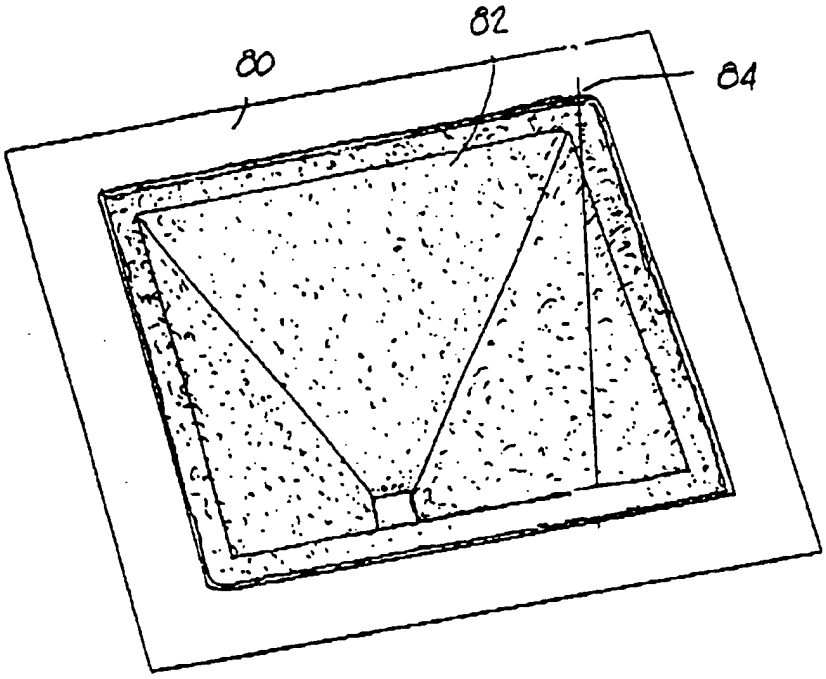


FIG.3A

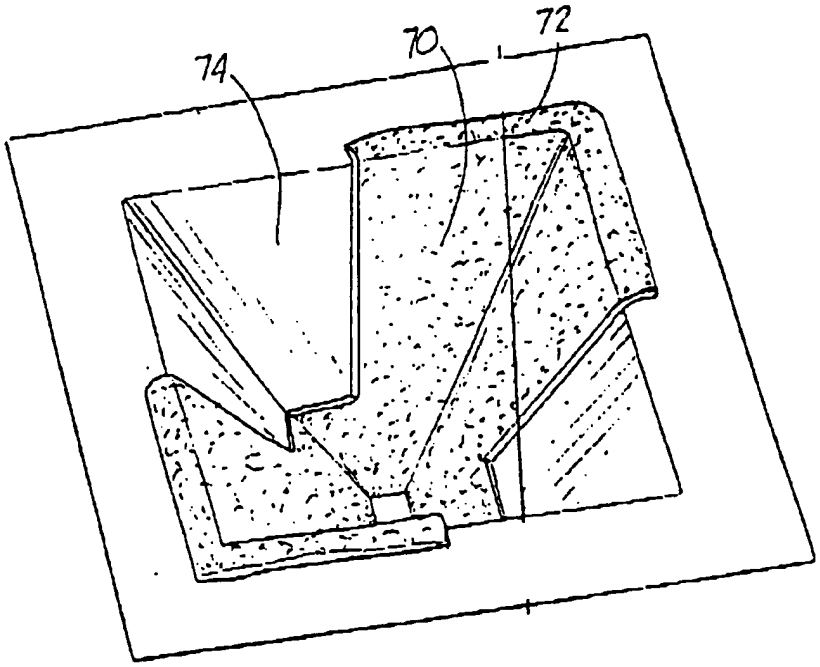


FIG.3B

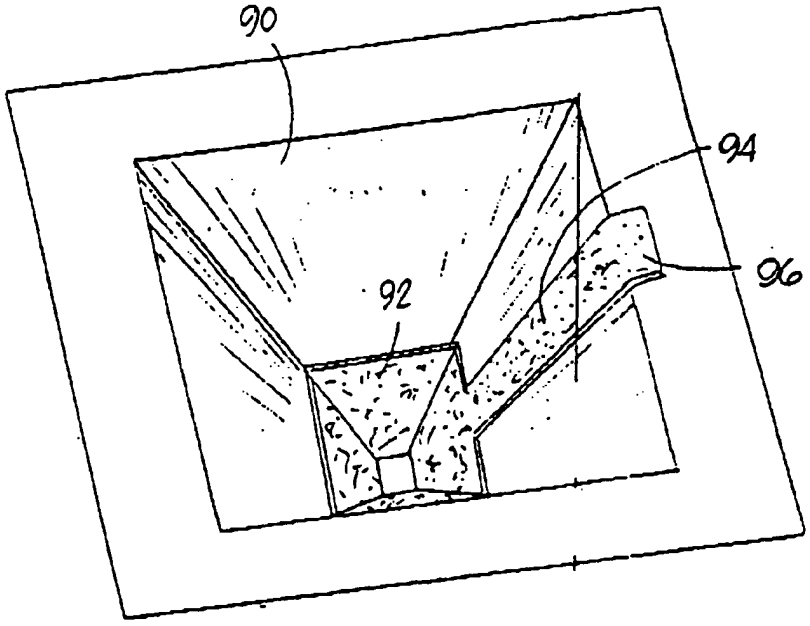


FIG. 3C

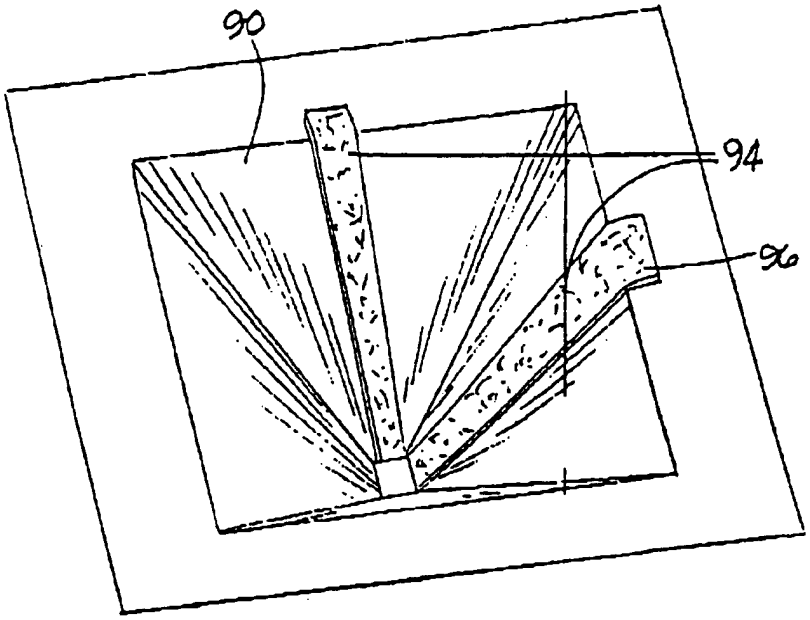


FIG. 3D

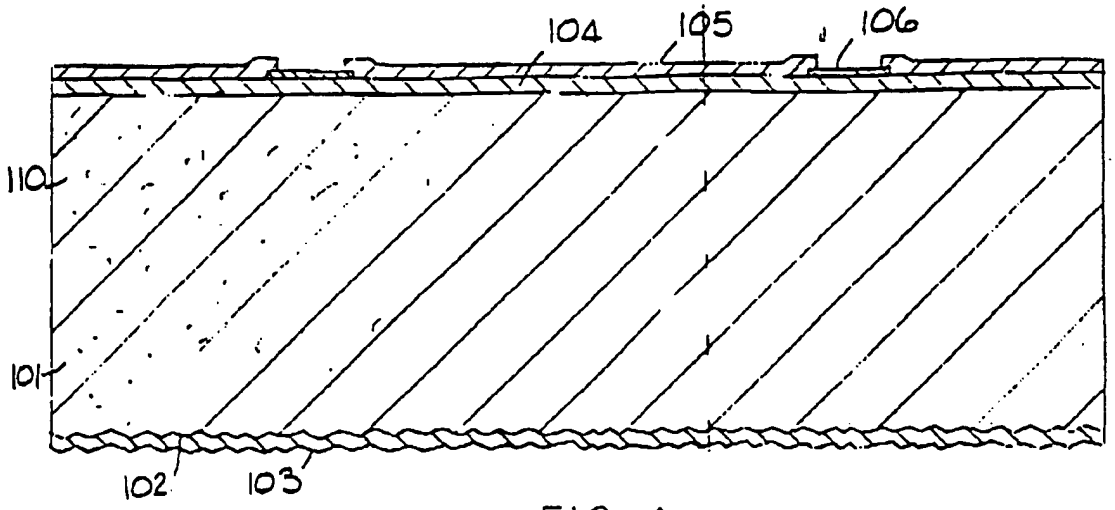


FIG.4A

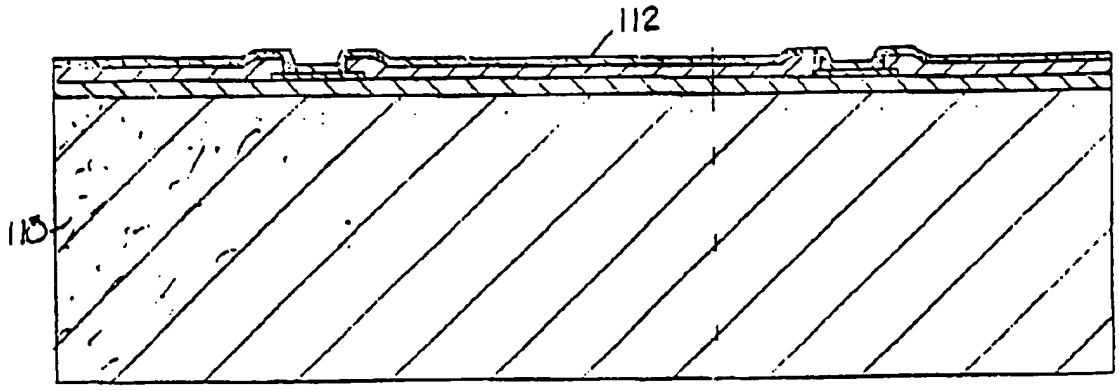


FIG.4B

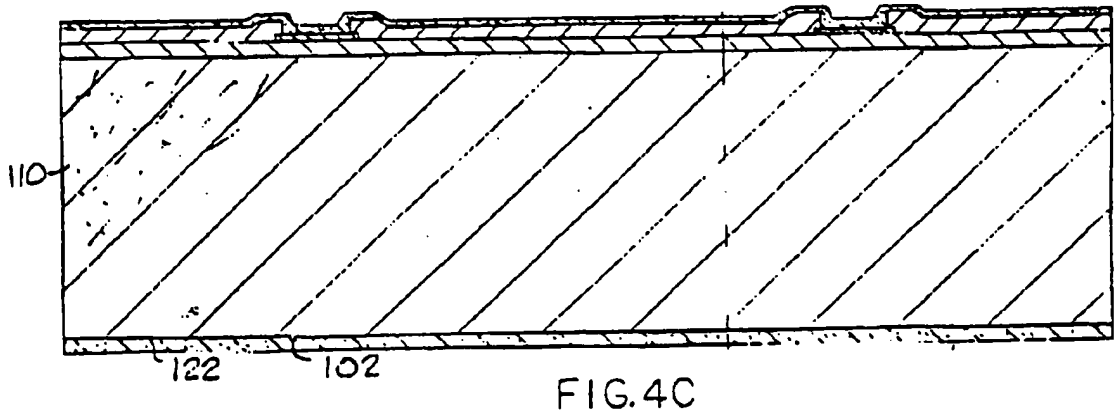


FIG.4C

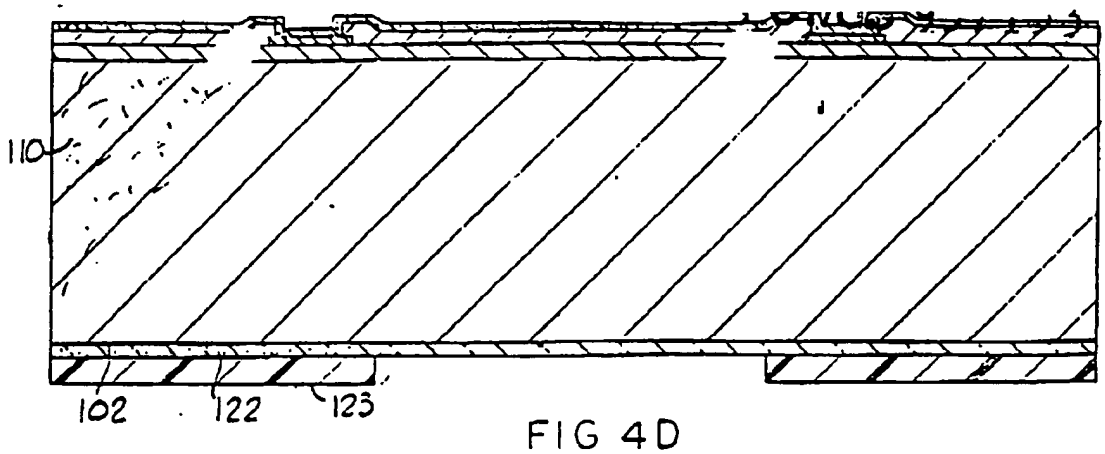


FIG 4D

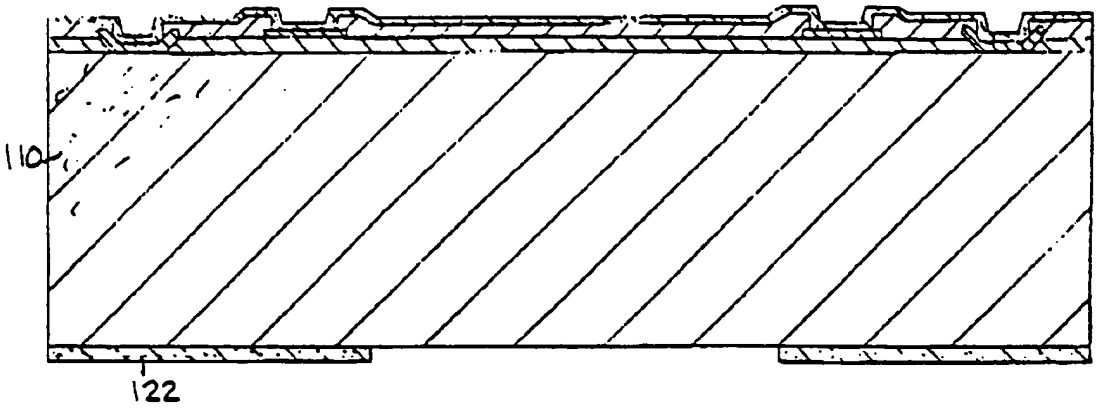


FIG. 4E

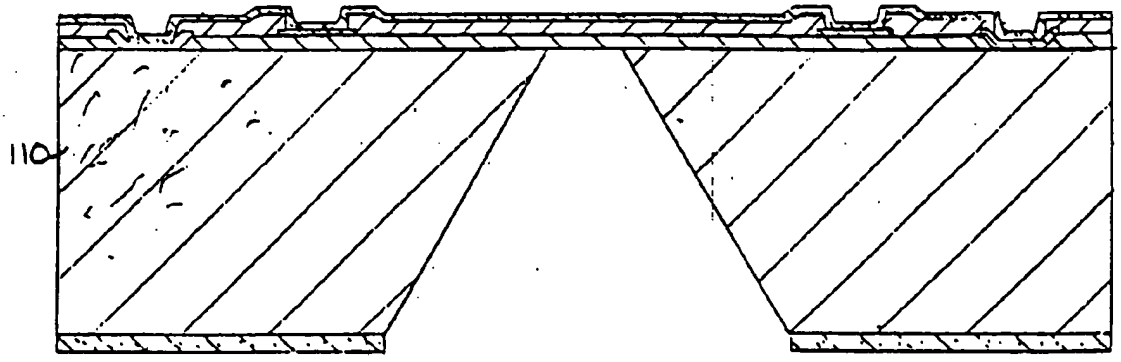


FIG. 4F

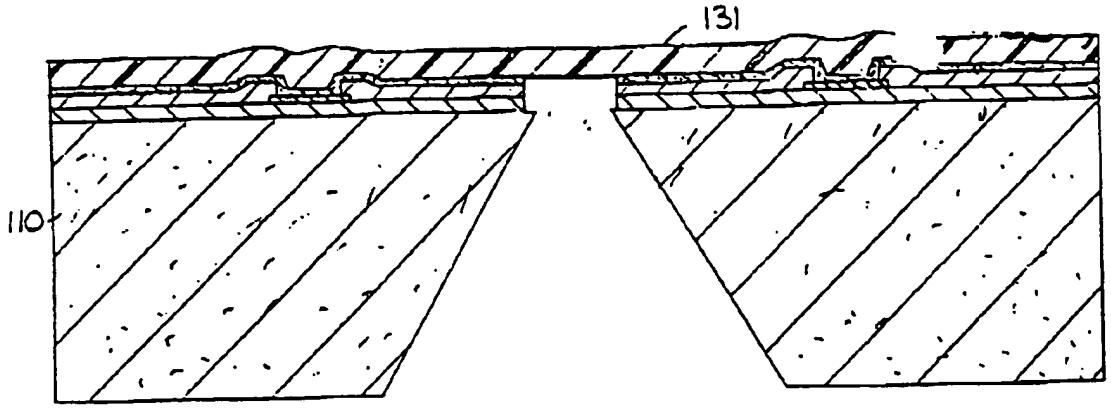


FIG.4G

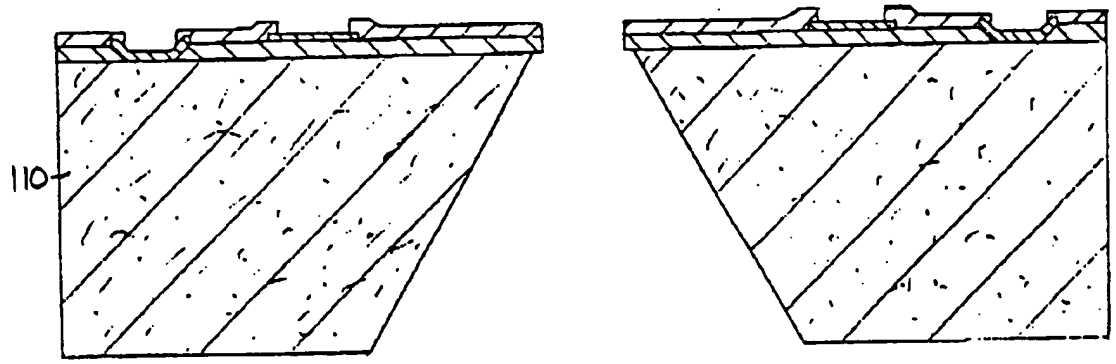


FIG.4H

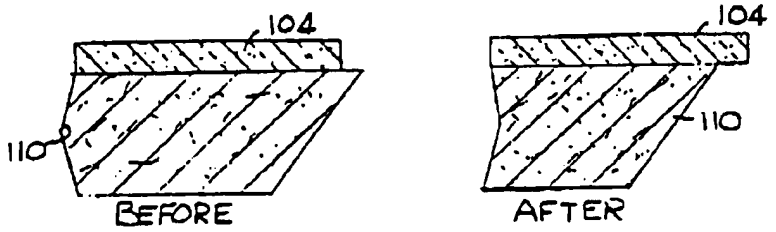


FIG.4I

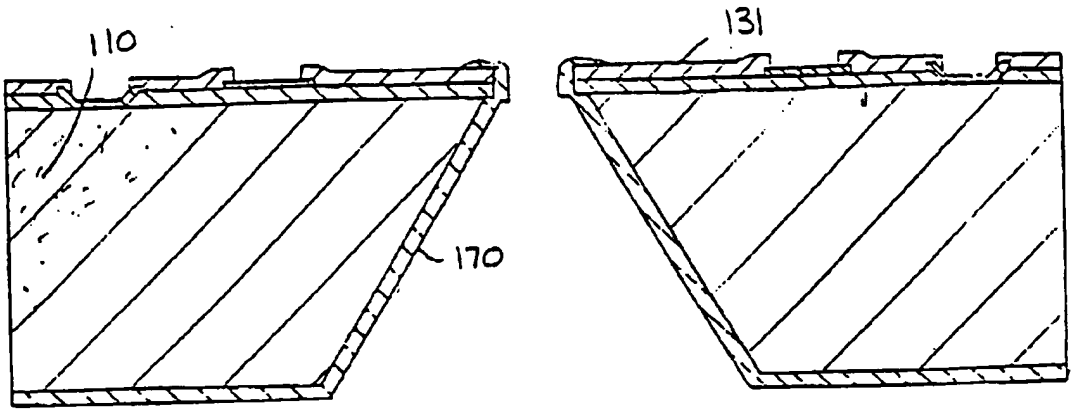


FIG.4J

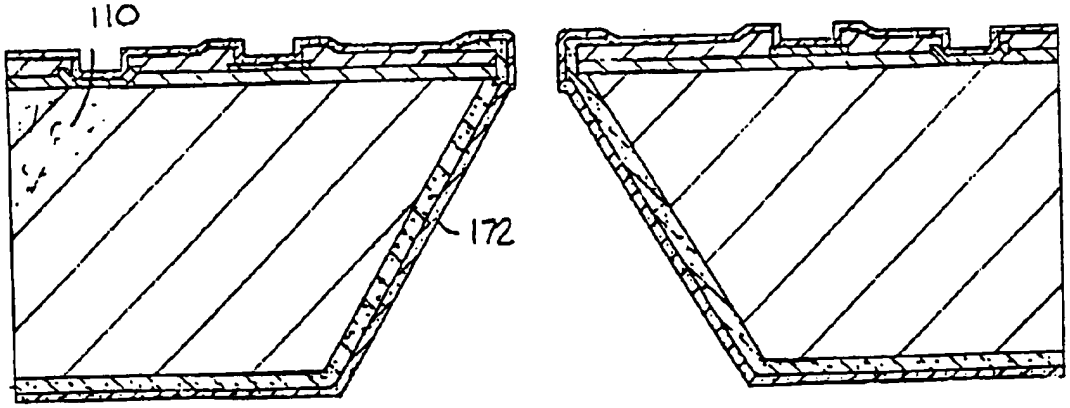


FIG.4K

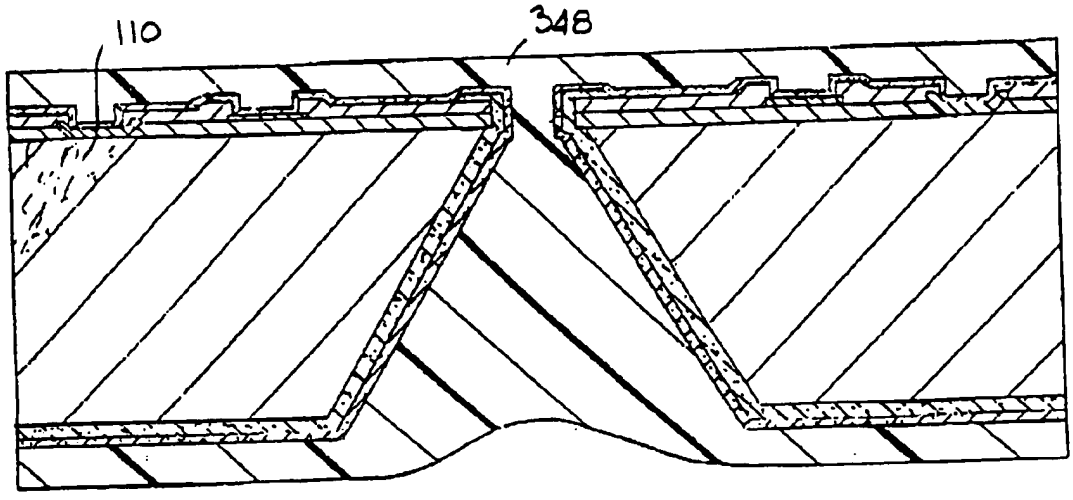


FIG.4L

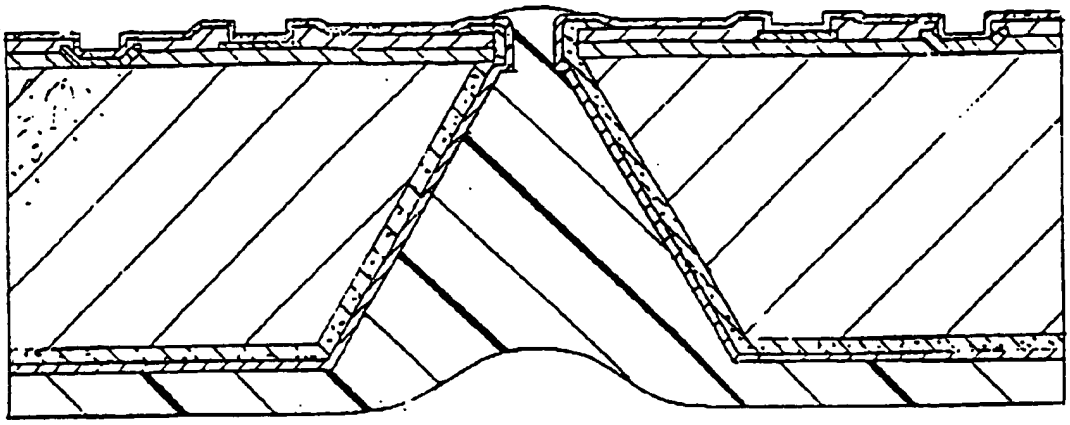


FIG. 4M

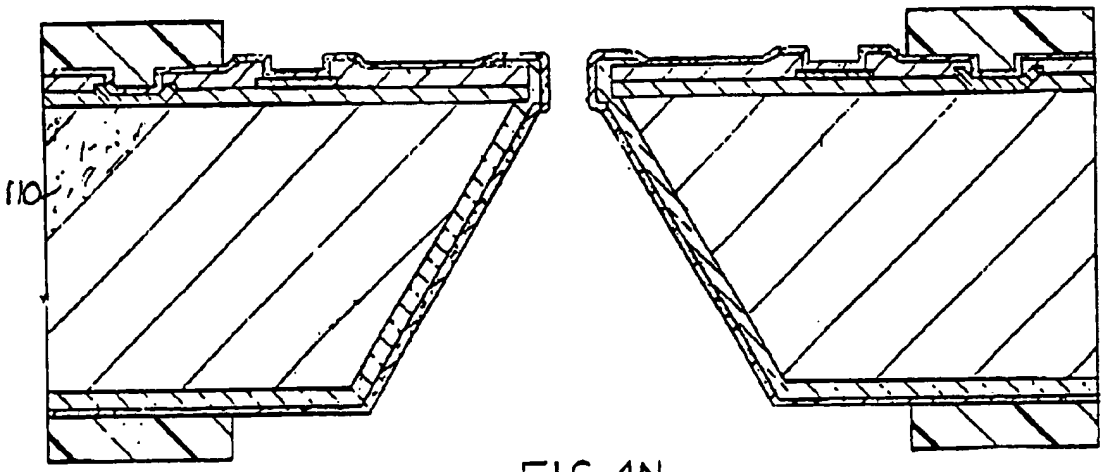


FIG. 4N

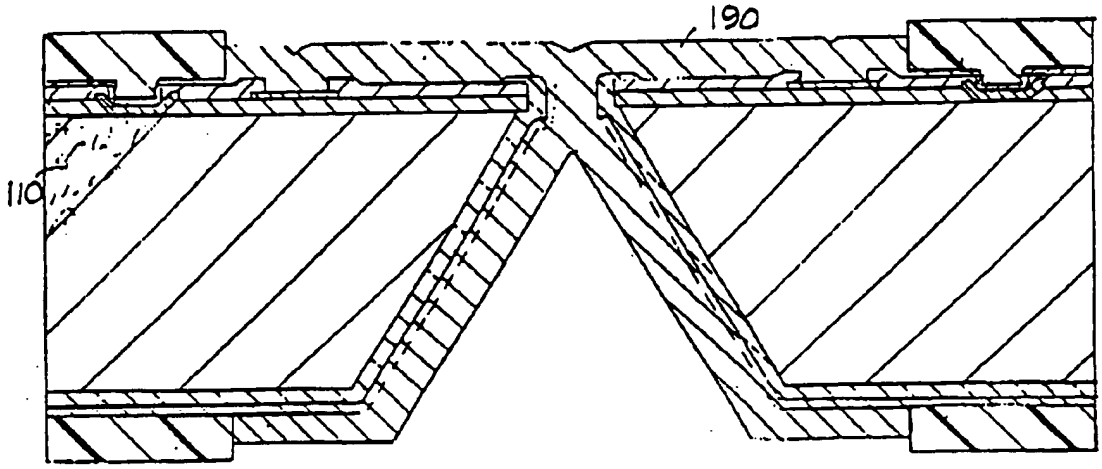


FIG. 4 O

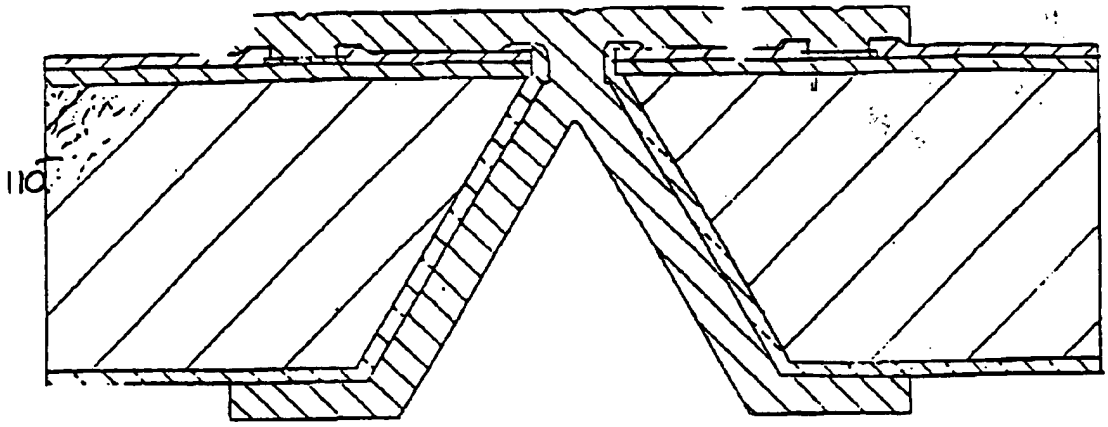


FIG.4P

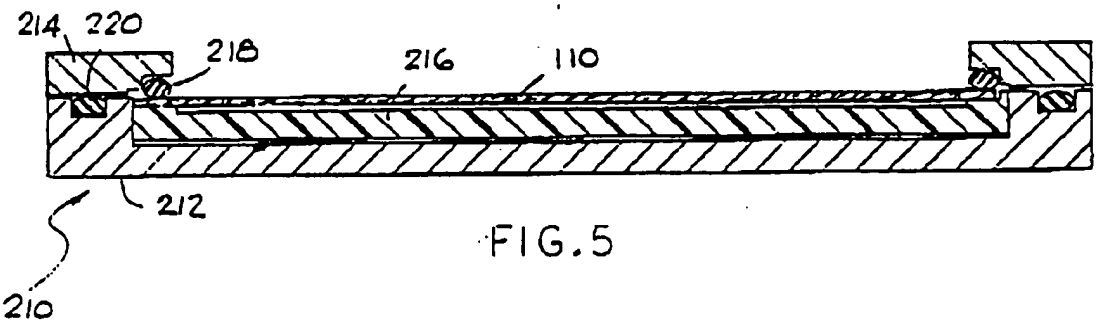


FIG.5

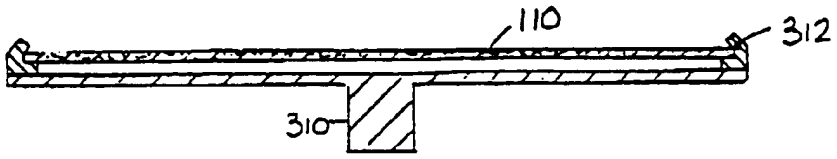


FIG.6